Amendments to the Specification:

Please replace paragraph [0030] as filed (paragraph [0032] as published) with the following amended paragraph:

[0030] In the above, the operating frequency decision unit 310 generates a ~~high frequency~~ detecting signal (HF) depending on the operating frequency (for example, the frequency of the external clock signal) of the semiconductor memory device 300. If the external clock signal (Ext_CLK) corresponds to the HF since it is higher than a given frequency, the operating frequency decision unit 310 activates the HF (defined as a Low level in the present embodiment). The internal clock signal generator 320 waveform-shapes the external clock signal (Ext_CLK) depending on the ~~high frequency~~ detecting signal (HF) to generate the internal clock signal (Int_CLK), or generates the external clock signal (Ext_CLK) as the internal clock signal (Int_CLK) as it is. At this time, if the external clock signal (Ext_CLK) corresponds to a low frequency, the internal clock signal generator 320 waveform-shapes the external clock signal (Ext_CLK) to generate the internal clock signal (Int_CLK). If the external clock signal (Ext_CLK) corresponds to the high frequency, the internal clock signal generator 320 generates the external clock signal (Ext_CLK) as the internal clock signal (Int_CLK) as it is. Meanwhile, the waveform shaping of the external clock signal (Ext_CLK) can be accomplished by logically combining the external clock signal (Ext_CLK) and the delay signal (A) of the external clock signal (Ext_CLK).

Please replace paragraph [0032] as filed (paragraph [0034] as published) with the following amended paragraph:

[0032] For example, before the memory device 300 is operated, a mode ~~resister~~ register set command (MRS command) including signals such as a burst length, a burst type, a column address strobe (CAS) latency and an operating mode is inputted from an external chip set 200, thus deciding the operating mode of the memory device 300. The MRS command is stored at a mode register 330 provided in the memory device 300. At this time, whether the ~~high frequency~~ detecting signal (HF) has been activated may be decided on the basis of the data for the CAS latency of the MRS command that is inputted from the external chip set 200 and stored at the mode register 330. The CAS latency indicates time latency from a command to output data of a given page is issued until the output is actually performed when any memory cell (page or address block) is activated.

Please replace paragraph [0034] as filed (paragraph [0036] as published) with the following amended paragraph:

[0034] For example, if the data for the CAS latency is over 4 (100 to 111), it may be set to activate the ~~high frequency~~ detecting signal (HF) considering that the external clock signal is the high frequency. In this case, if the data for the CAS latency is over 4 bit, the most significant bit (CL<2>) is always '1' of the data of the 3 bits (CL<0> to CL<2>). Thus, as shown in FIG. 4, the operating frequency decision unit 310 can be implemented only using an inverter I310 for inverting the level of the most significant bit (CL<2>) so that the ~~high frequency~~ detecting signal (HF) becomes activated (Low level) only when the most significant bit is '1' as a result of sensing only the most significant bit (CL<2>).

[[□]] Table 1[[□]]

CL<2>	CL<1>	CL<0>	CL Data Value
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Please replace paragraph [0035] as filed (paragraph [0037] as published) with the following amended paragraph:

[0035] For example, in case that the ~~high frequency~~ detecting signal (HF) is outputted by sensing only the data value of the most significant bit (CL<2>), it is possible to implement the operating frequency decision unit 310 using only the inverter for inverting the data of the most significant bit (CL<2>).

Please replace paragraph [0037] as filed (paragraph [0039] as published) with the following amended paragraph:

[0037] Meanwhile, though not shown in the drawings, a frequency sensing means (not shown) of the external clock signal (Ext_CLK) may be located within the memory device

300. The frequency sensing means compares the frequency of the external clock signal (Ext_CLK) that is externally inputted with the basic frequency to determine whether the frequency of the external clock signal is the high frequency or the low frequency and may activate the ~~high frequency~~ detecting signal (HF) only when the external clock signal is the high frequency as a result of the determination.

Please replace paragraph [0038] as filed (paragraph [0040] as published) with the following amended paragraph:

[0038] The internal clock signal generator 320 generates the internal clock signal (Int_CLK) using the external clock signal (Ext_CLK) and, it is determined whether to generate the internal clock signal (Int_CLK) for the low frequency by transforming the external clock signal (Ext_CLK) depending on the ~~high frequency~~ detecting signal (HF), or to use the external clock signal (Ext_CLK) as the internal clock signal (Int_CLK) for the high frequency as it is.

Please replace paragraph [0039] as filed (paragraph [0041] as published) with the following amended paragraph:

[0039] Such internal clock signal generator 320 may include a delay unit D320 for delaying the external clock signal (Ext_CLK) by some time to generate the delay signal (A), and a pulse-shaping unit P320 for logically combining the external clock signal (Ext_CLK) and the delay signal (A) to generate the internal clock signal (Int_CLK) for the low frequency or transmit the external clock signal (Ext_CLK) as the internal clock signal (Int_CLK) for the high frequency as it is if the ~~high frequency~~ detecting signal (HF) is activated.

Please replace paragraph [0042] as filed (paragraph [0044] as published) with the following amended paragraph:

[0042] Meanwhile, the pulse-shaping unit P320 may include a first logical means N321 to which the external clock signal (Ext_CLK), the delay signal (A) and the ~~high frequency~~ detecting signal (HF) are inputted, and a second logical means N322 to which the external clock signal (Ext_CLK) and the output signal of the first logical means N321 are inputted. At this time, if the first logical means N321 or the second logical means N322 consists of a NAND gate, an inverter I321 for inverting the output signal of the second logical means

N322 is further installed at the output terminal of the second logical means N322. Meanwhile, though only a single logical means N322 is installed between the first logical means N321 and the inverter I312 in the drawing, the number of the logical means N322 may be different depending on the case.

Please replace paragraph [0043] as filed (paragraph [0045] as published) with the following amended paragraph:

[0043] How the internal clock signal generator 320 constructed above operates depending on the ~~high frequency~~ detecting signal (HF) will now be descried with reference to the waveform. At this time, if the external clock signal is a low frequency, since the ~~high frequency~~ detecting signal (HF) is generated as a High level (inactive) and thus does not give influence on the operation of the first logical means N321, the internal waveform of the internal clock signal generator 320 is same as that of FIGs. 2A and 2B. At this time, the internal clock signal (Int_CLK) ~~generated becomes the internal clock signal (Int_CLK) for the low frequency~~ is used when the external clock signal (Ext CLK) is the low frequency. The internal clock signal (Int CLK) ~~for the low frequency has the same pulse width as those of the external clock signal but~~ has a pulse width corresponding to the delay time of ~~the delay signal for the external clock signal~~ the delay unit D320.

Please replace paragraph [0044] as filed (paragraph [0046] as published) with the following amended paragraph:

[0044] However, if the external clock signal corresponds to a high frequency and the ~~high frequency~~ detecting signal (HF) is thus activated as a Low level, they operate quite differently. FIG. 6 show internal waveforms for explaining the process of generating the pulse in the circuit for generating the internal clock signal shown in FIG. 3.